What is claimed is:

1 An out-of-sync detector that detects whether or not two signals are synchronized with each other, comprising:

a first circuit for delaying one of said two signals by a predetermined phase and outputting a delayed signal;

a second circuit for sampling outputs of said first circuit in sync with a transition of the other of said two signals;

a third circuit for outputting an average value of an output from said second circuit; and

a fourth circuit for comparing said average value with a predetermined threshold value and detecting the presence or absence of out-of-synchronization.

2 An out-of-sync detector, which receives a first signal and a second signal of which the phase and frequency are synchronized with those of said first signal and detects whether or not said first signal is synchronized with said second signal, comprising:

a delay circuit for delaying said second signal by a predetermined phase;

a sequential logical circuit for sampling said second signal delayed by said delay circuit, in sync with a

falling or rising transition of said second signal;

an average value detector for detecting an average value of an output of said sequential logical circuit; and

a comparator for comparing in amplitude the average value from said average value detector with a predetermined threshold value and then outputting a comparison result as a signal indicating the presence or absence of out-of-synchronization.

3 The out-of-sync detector defined in Claim 2, wherein said second signal comprises an oscillation output signal of a signal oscillator, said signal oscillator receiving a control signal having a value corresponding to a difference in frequency and phase between said first signal and said second signal and varying its oscillation frequency under said control signal.

4 The out-of-sync detector defined in Claim 2, wherein said delay circuit delays said second signal by a phase component corresponding to a half of the pulse width of said second signal.

5 An out-of-sync detector comprising:

a delay circuit for delaying a clock from a signal

oscillator by a predetermined phase, the oscillation frequency of said signal oscillator being varied by a control signal;

a flip-flop for sampling a clock delayed by the said delay circuit, at a falling edge or rising edge of a data signal;

an average value detector for detecting and outputting an average of an output from said flip-flop; and

a comparator for comparing said average value with a predetermined threshold value and issuing an alarm at the time of detecting out-of-synchronization.

6 The out-of-sync detector defined in Claim 5 wherein said signal oscillator comprises a voltage controlled oscillator or a current controlled oscillator, said voltage controlled oscillator or said current controlled oscillator receiving a control signal in accordance with a difference in frequency and in phase output from said phase frequency comparator, oscillating at an oscillation frequency in accordance with said control signal, and thus outputting an oscillation clock, said phase frequency comparator receiving said received data and said clock.

7 The out-of-sync detector defined claim 5, wherein said delay circuit delays said clock by a phase amount

corresponding to a half of a pulse width of said clock.

8 The out-of-sync detector defined in Claim 6, wherein said delay circuit outputs a clock of which the frequency or phase is delayed by 90 degrees.

9 The out-of-sync detector defined in Claim 5, wherein said average value output from said average value detector has a first value when said data signal is synchronized with said clock in frequency and in phase, with said clock falling in sync with transition of said data signal; and wherein said comparator detects an increase in jitter of said data signal and produces said alarm when said average value is smaller than a predetermined threshold value, said predetermined threshold value being set between said first value and an intermediate value, said intermediate value being set between said first value and a second value smaller than said first value.

10 The out-of-sync detector defined in Claim 5, wherein said average value output from said average value detector has a first value when said data signal is synchronized with said clock in frequency and in phase, with said clock rising in sync with transition of said data signal; and wherein said comparator issues said alarm when said

average value is equal to or smaller than a threshold value, said threshold value being set to an intermediate value between said first value and a second value smaller than said first value.

11 The out-of-sync detector defined in Claim 5, wherein said average value output from said average value detector has a second value when said data signal is synchronized with said clock pulse in frequency and in phase, said clock pulse rising in sync with transition of said data signal; and wherein said comparator detects an increase in jitter of said data signal when said average value is larger than a predetermined threshold value and then issues said alarm, said predetermined threshold value being set between said second value and an intermediate value, said intermediate value being between said second value and a first value larger than said second

value, said intermediate value being set between said second value and a first value larger than said second value.

13 The out-of-sync detector defined in Claim 5, wherein said average value detector creates a dc voltage corresponding to an average value obtained by averaging an output value of said flip-flop with respect to time for a predetermined time period, and then outputting said dc voltage as said average value.

14 The out-of-sync detector defined in Claim 5, wherein said average value detector outputs as said average value a dc voltage between a first value and a second value, said dc voltage representing a ratio at which the sum of time widths occupies for a predetermined period, each of said time widths in which an output of said flip-flop has a first value or a second value.

15 A receiver comprising:

a first circuit for delaying one of said two signals by a predetermined phase and outputting a delayed signal;

a second circuit for sampling outputs of said first circuit in sync with a transition of the other of

said two signals;

a third circuit for outputting an average value of an output from said second circuit; and

a fourth circuit for comparing said average value with a predetermined threshold value and detecting the presence or absence of out-of-synchronization.

16 A receiver comprising:

a receiving circuit for receiving a first signal and a second signal of which the phase and frequency are synchronized with those of said first signal;

a delay circuit for delaying said second signal by a predetermined phase;

a sequential logical circuit for sampling said second signal delayed by said delay circuit, in sync with a falling or rising transition of said second signal;

an average value detector for detecting an average value of an output of said sequential logical circuit; and

a comparator for comparing in amplitude the average value from said average value detector with a predetermined threshold value and then outputting a comparison result as a signal indicating the presence or absence of out-of-synchronization.

16
17 The receiver defined in Claim 16, wherein said second signal comprises an oscillation output signal of a signal oscillator, said signal oscillator receiving a control signal having a value corresponding to a difference in frequency and phase between said first signal and said second signal and varying its oscillation frequency under said control signal.

17
18 The receiver defined in Claim 16, wherein said delay circuit delays said second signal by a phase component corresponding to a half of the pulse width of said second signal.

18
19 A receiver comprising:

a delay circuit for delaying a clock from a signal oscillator by a predetermined phase, the oscillation frequency of said signal oscillator being varied by a control signal;

a flip-flop for sampling a clock delayed by the said delay circuit, at a falling edge or rising edge of a data signal;

an average value detector for detecting and outputting an average of an output from said flip-flop; and

a comparator for comparing said average value with a predetermined threshold value and issuing an alarm at

the time of detecting out-of-synchronization.

19
20 The receiver defined in Claim 19 wherein said signal oscillator comprises a voltage controlled oscillator or a current controlled oscillator, said voltage controlled oscillator or said current controlled oscillator receiving a control signal in accordance with a difference in frequency and in phase output from said phase frequency comparator, oscillating at an oscillation frequency in accordance with said control signal, and thus outputting an oscillation clock, said phase frequency comparator receiving said received data and said clock.

20
21 The receiver defined claim 19, wherein said delay circuit delays said clock by a phase amount corresponding to a half of a pulse width of said clock.

21
22 The receiver defined in Claim 20, wherein said delay circuit outputs a clock of which the frequency or phase is delayed by 90 degrees.

22
23 The receiver defined in Claim 19, wherein said average value output from said average value detector has a first value when said data signal is synchronized with said clock in frequency and in phase, with said clock

falling in sync with transition of said data signal; and wherein said comparator detects an increase in jitter of said data signal and produces said alarm when said average value is smaller than a predetermined threshold value, said predetermined threshold value being set between said first value and an intermediate value, said intermediate value being set between said first value and a second value smaller than said first value.

24 The receiver defined in Claim 19, wherein said average value output from said average value detector has a first value when said data signal is synchronized with said clock in frequency and in phase, with said clock rising in sync with transition of said data signal; and wherein said comparator issues said alarm when said average value is equal to or smaller than a threshold value, said threshold value being set to an intermediate value between said first value and a second value smaller than said first value.

25 The receiver defined in Claim 19, wherein said average value output from said average value detector has a second value when said data signal is synchronized with said clock pulse in frequency and in phase, said clock pulse rising in sync with transition of said data signal;

and wherein said comparator detects an increase in jitter of said data signal when said average value is larger than a predetermined threshold value and then issues said alarm, said predetermined threshold value being set between said second value and an intermediate value, said intermediate value being between said second value and a first value larger than said second value.

26 The receiver defined in Claim 19, wherein said average value output from said average value detector has a second value when said data signal is synchronized with said clock in frequency and in phase, with said clock rising in sync with transition of said data signal; and wherein said comparator issues said alarm when said average value is equal to or larger than an intermediate value, said intermediate value being set between said second value and a first value larger than said second value.

27 The receiver defined in Claim 19, wherein said average value detector creates a dc voltage corresponding to an average value obtained by averaging an output value of said flip-flop with respect to time for a predetermined time period, and then outputting said dc voltage as said average value.

27

28 The receiver defined in Claim 19, wherein said average value detector outputs as said average value a dc voltage between a first value and a second value, said dc voltage representing a ratio at which the sum of time widths occupies for a predetermined period, each of said time widths in which an output of said flip-flop has a first value or a second value.

28

29 An optical receiver comprising:

a delay circuit for delaying a clock from a signal oscillator by a predetermined phase, the oscillation frequency of said signal oscillator being varied by a control signal;

a flip-flop for sampling a clock delayed by the said delay circuit, at a falling edge or rising edge of a data signal detected by an optical detector;

an average value detector for detecting and outputting an average of an output from said flip-flop; and

a comparator for comparing said average value with a predetermined threshold value and issuing an alarm at the time of detecting out-of-synchronization.

29

30 The optical receiver defined in Claim 29 wherein said signal oscillator comprises a voltage controlled

oscillator or a current controlled oscillator, said voltage controlled oscillator or said current controlled oscillator receiving a control signal in accordance with a difference in frequency and in phase output from said phase frequency comparator, oscillating at an oscillation frequency in accordance with said control signal, and thus outputting an oscillation clock, said phase frequency comparator receiving said received data and said clock.

30
31 The optical receiver defined claim 29, wherein said delay circuit delays said clock by a phase amount corresponding to a half of a pulse width of said clock.

31
32 The optical receiver defined in Claim 30, wherein said delay circuit outputs a clock of which the frequency or phase is delayed by 90 degrees.

32
33 The optical receiver defined in Claim 29, wherein said average value output from said average value detector has a first value when said data signal is synchronized with said clock in frequency and in phase, with said clock falling in sync with transition of said data signal; and wherein said comparator detects an increase in jitter of said data signal and produces said alarm when said average value is smaller than a predetermined threshold value,

said predetermined threshold value being set between said first value and an intermediate value, said intermediate value being set between said first value and a second value smaller than said first value.

33
34 The optical receiver defined in Claim 29, wherein said average value output from said average value detector has a first value when said data signal is synchronized with said clock in frequency and in phase, with said clock rising in sync with transition of said data signal; and wherein said comparator issues said alarm when said average value is equal to or smaller than a threshold value, said threshold value being set to an intermediate value between said first value and a second value smaller than said first value.

34
35 The optical receiver defined in Claim 29, wherein said average value output from said average value detector has a second value when said data signal is synchronized with said clock pulse in frequency and in phase, said clock pulse rising in sync with transition of said data signal; and wherein said comparator detects an increase in jitter of said data signal when said average value is larger than a predetermined threshold value and then issues said alarm, said predetermined threshold value

being set between said second value and an intermediate value, said intermediate value being between said second value and a first value larger than said second value.

35
36 The out-of-sync detector defined in Claim 29, wherein said average value output from said average value detector has a second value when said data signal is synchronized with said clock in frequency and in phase, with said clock rising in sync with transition of said data signal; and wherein said comparator issues said alarm when said average value is equal to or larger than an intermediate value, said intermediate value being set between said second value and a first value larger than said second value.

36
37 The optical receiver defined in Claim 29, wherein said average value detector creates a dc voltage corresponding to an average value obtained by averaging an output value of said flip-flop with respect to time for a predetermined time period, and then outputting said dc voltage as said average value.

37
38 The optical receiver defined in Claim 29, wherein said average value detector outputs as said average value a dc voltage between a first value and a second value,

said dc voltage representing a ratio at which the sum of time widths occupies for a predetermined period, each of said time widths in which an output of said flip-flop has a first value or a second value.

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